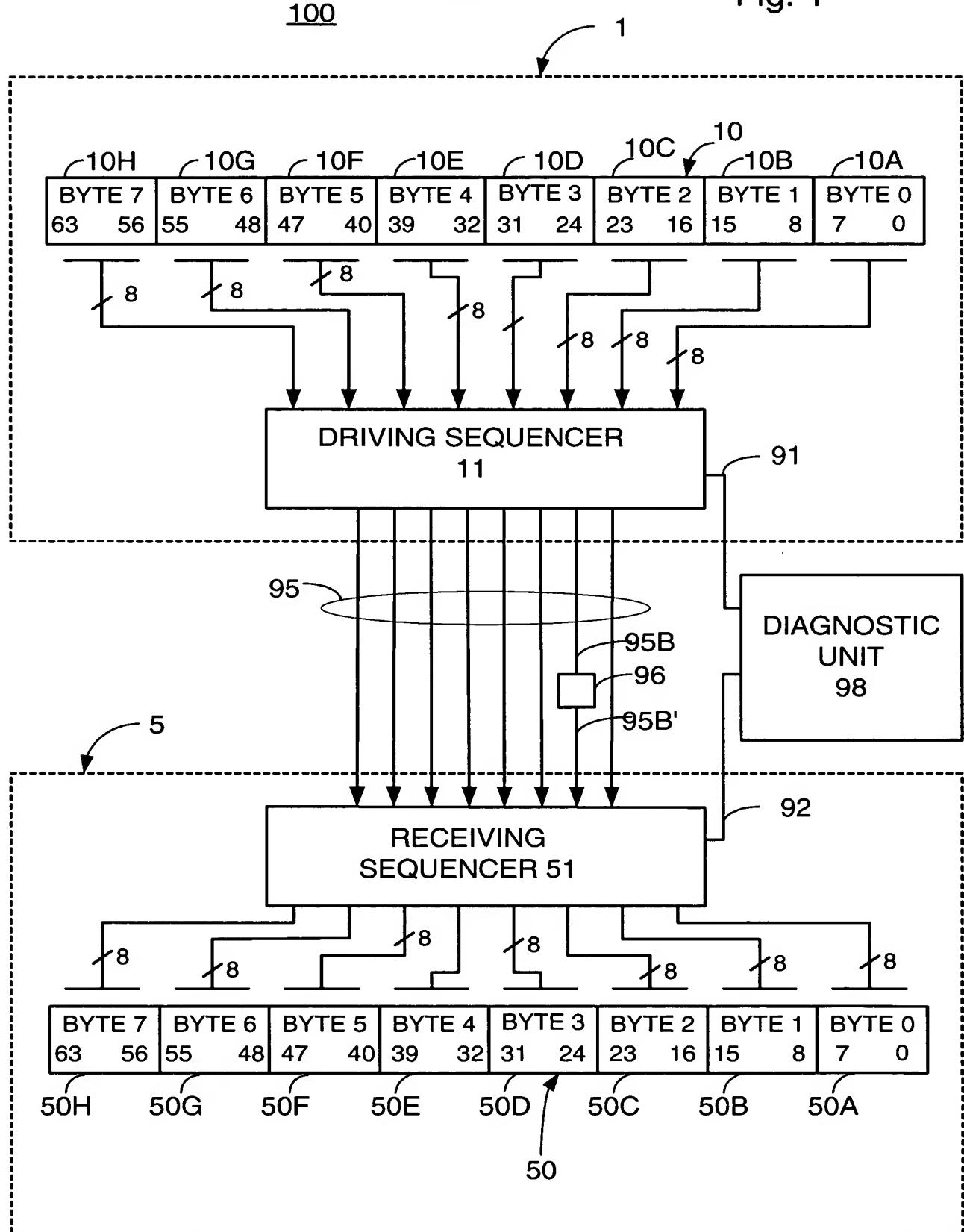


Fig. 1



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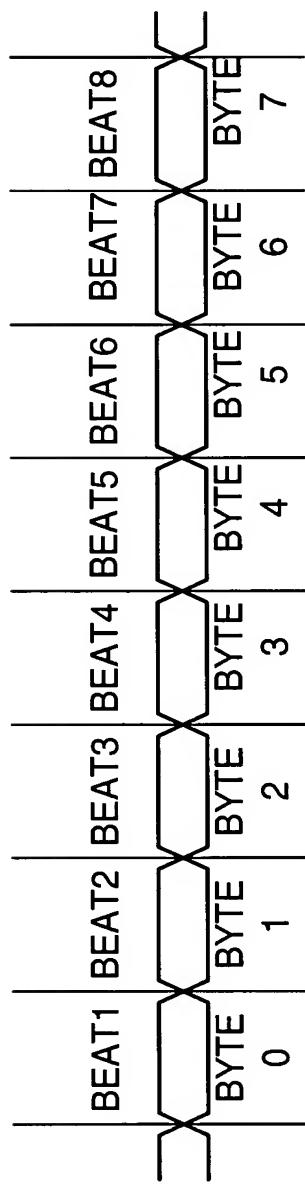


Fig. 2A

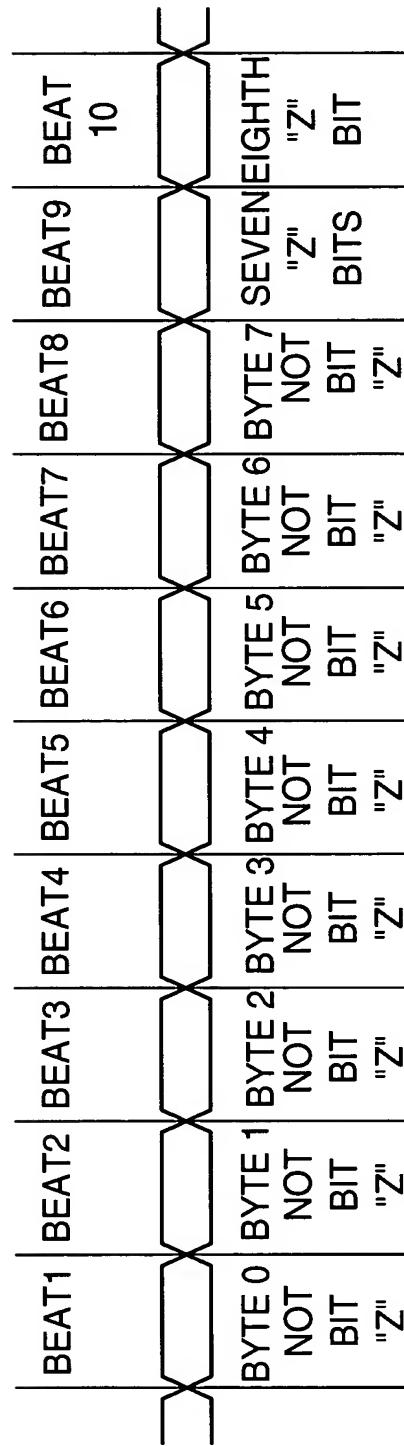


Fig. 2B

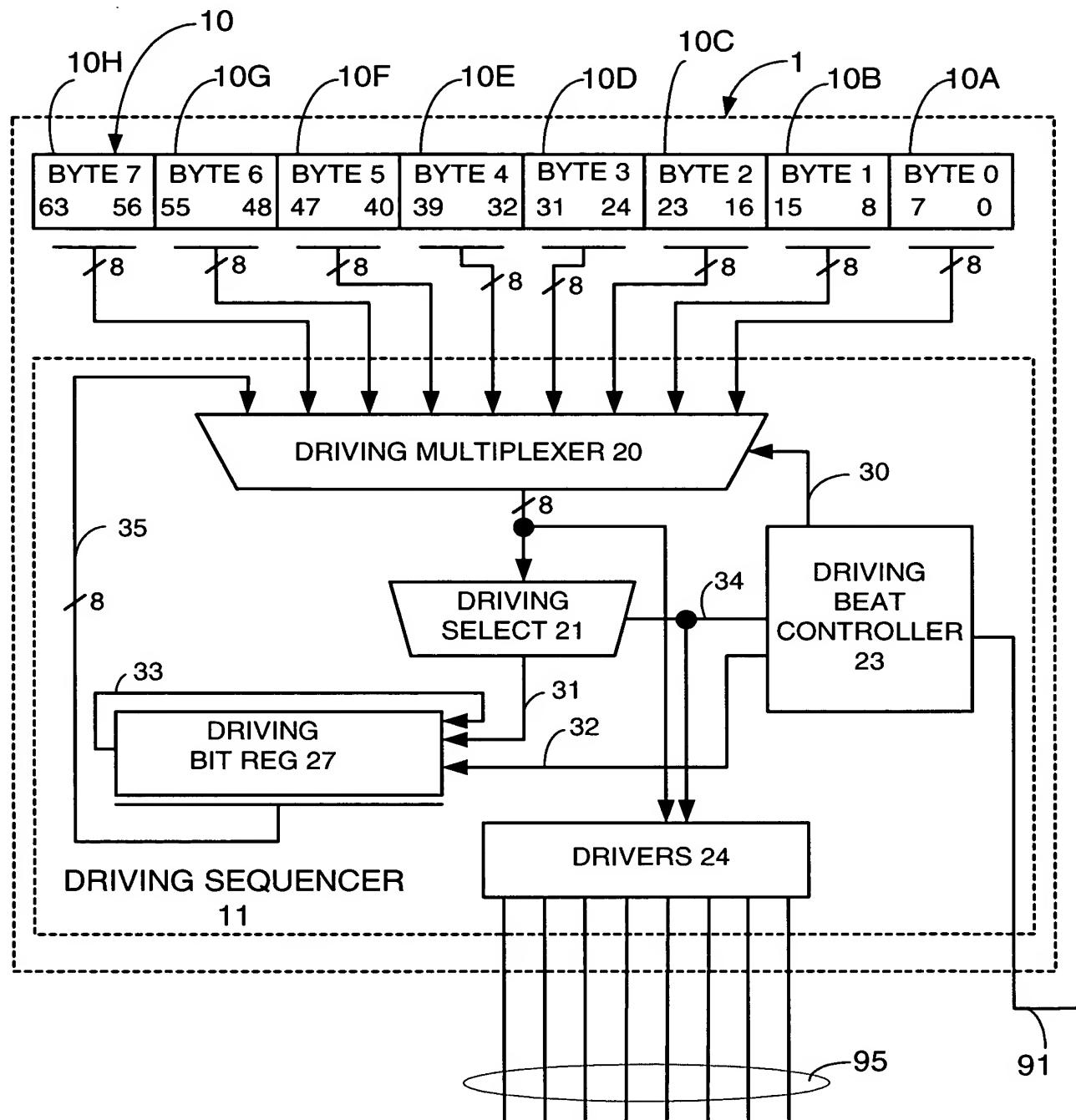


Fig. 3

PRE BEAT 1								
PRE BEAT 2								BYTE 0 BIT Z
PRE BEAT 3							BYTE 0 BIT Z	BYTE 1 BIT Z
PRE BEAT 4						BYTE 0 BIT Z	BYTE 1 BIT Z	BYTE 2 BIT Z
PRE BEAT 5					BYTE 0 BIT Z	BYTE 1 BIT Z	BYTE 2 BIT Z	BYTE 3 BIT Z
PRE BEAT 6				BYTE 0 BIT Z	BYTE 1 BIT Z	BYTE 2 BIT Z	BYTE 3 BIT Z	BYTE 4 BIT Z
PRE BEAT 7			BYTE 0 BIT Z	BYTE 1 BIT Z	BYTE 2 BIT Z	BYTE 3 BIT Z	BYTE 4 BIT Z	BYTE 5 BIT Z
PRE BEAT 8		BYTE 0 BIT Z	BYTE 1 BIT Z	BYTE 2 BIT Z	BYTE 3 BIT Z	BYTE 4 BIT Z	BYTE 5 BIT Z	BYTE 6 BIT Z
PRE BEAT 9	BYTE 0 BIT Z	BYTE 1 BIT Z	BYTE 2 BIT Z	BYTE 3 BIT Z	BYTE 4 BIT Z	BYTE 5 BIT Z	BYTE 6 BIT Z	BYTE 7 BIT Z
PRE BEAT 10	BYTE 1 BIT Z	BYTE 2 BIT Z	BYTE 3 BIT Z	BYTE 4 BIT Z	BYTE 5 BIT Z	BYTE 6 BIT Z	BYTE 7 BIT Z	BYTE 0 BIT Z

Fig. 4

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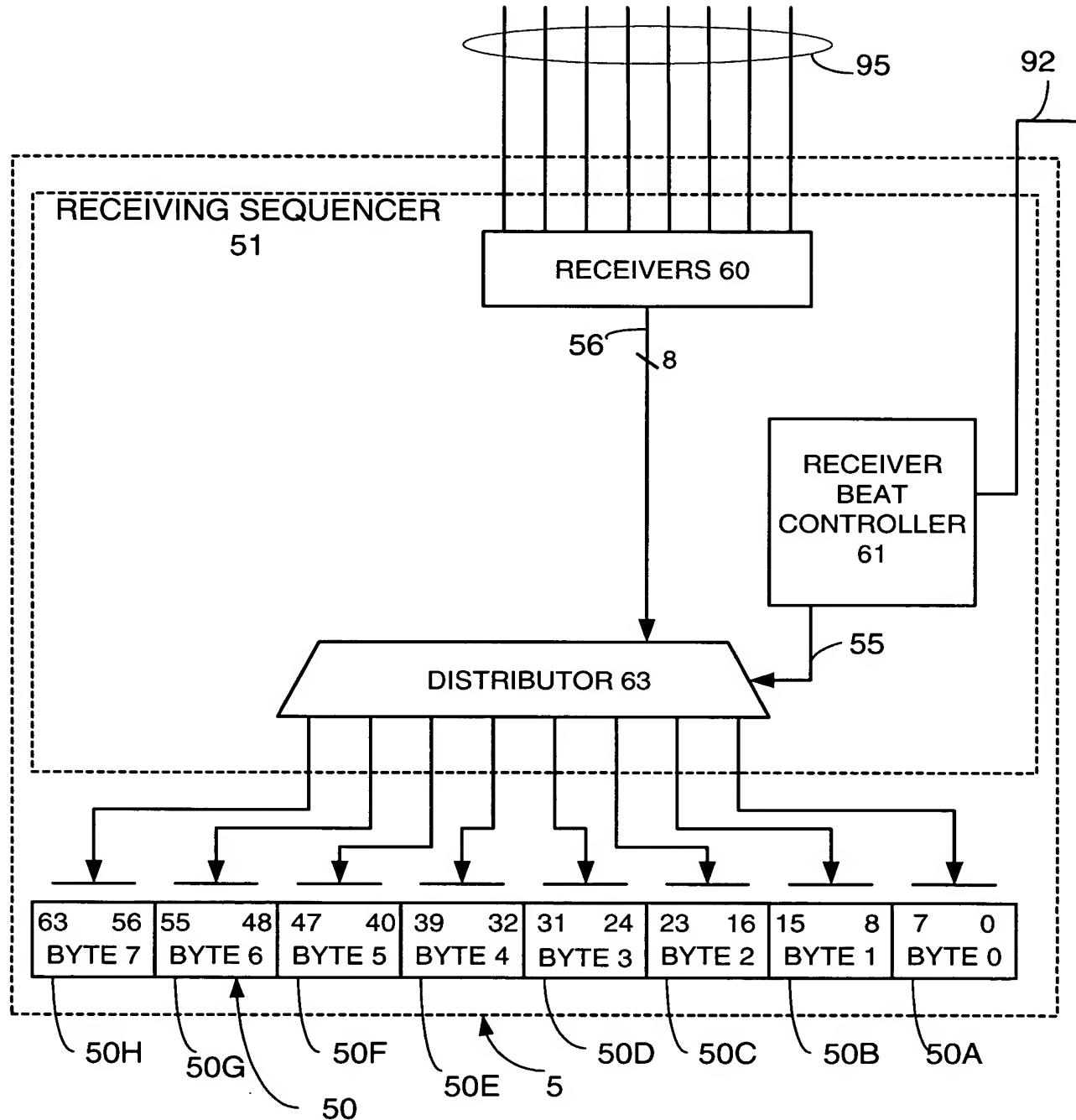


Fig. 5

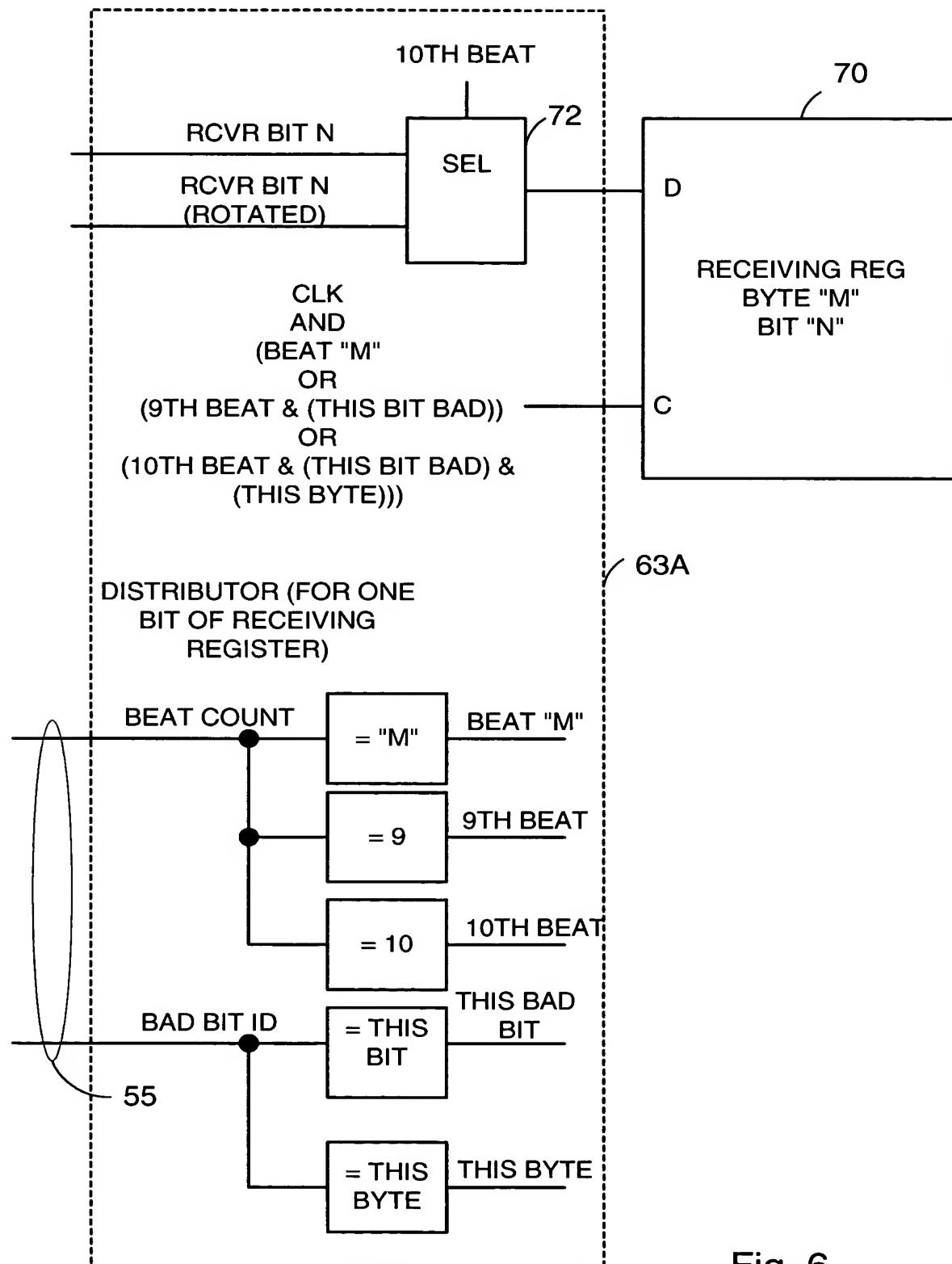
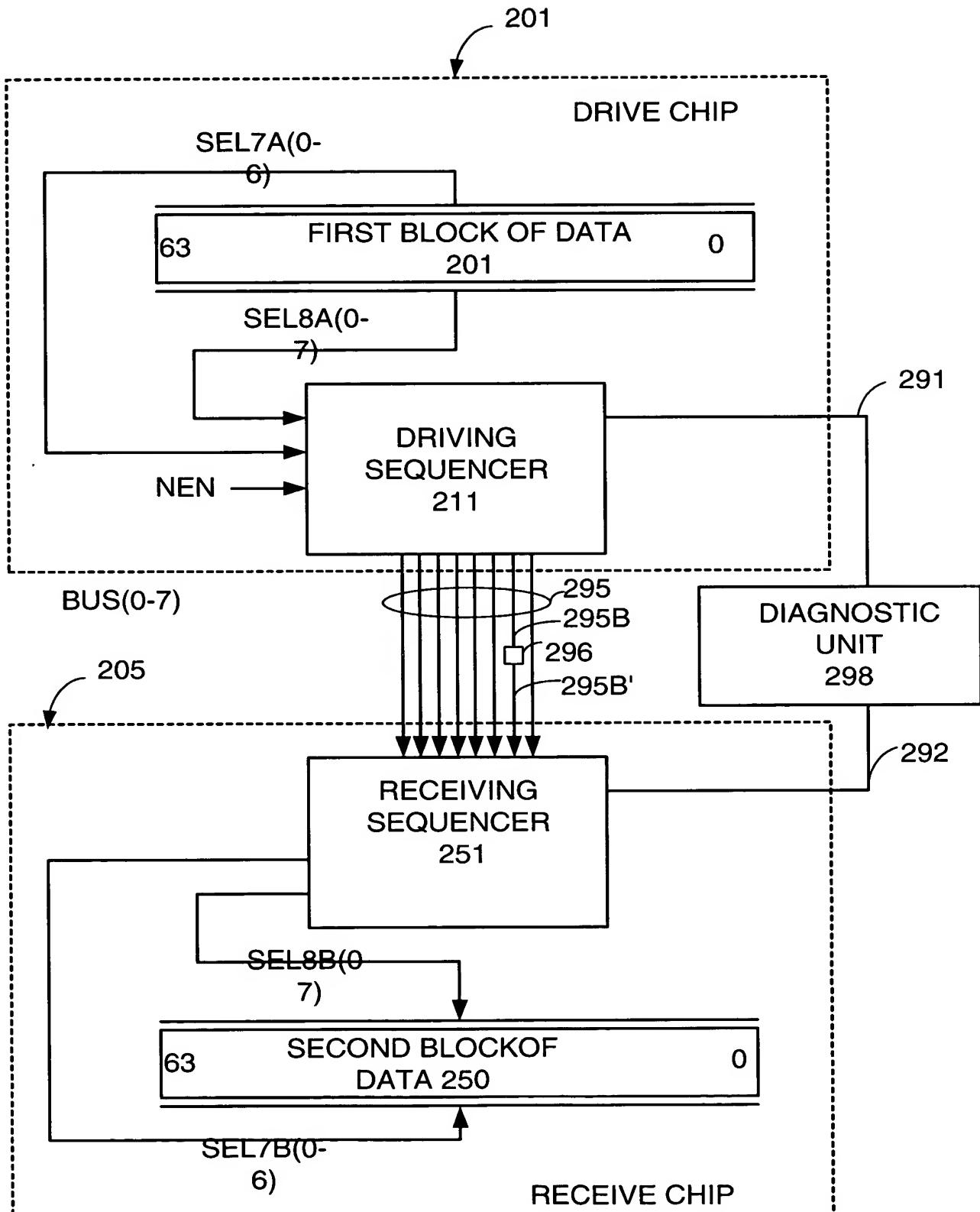


Fig. 6

Fig. 7



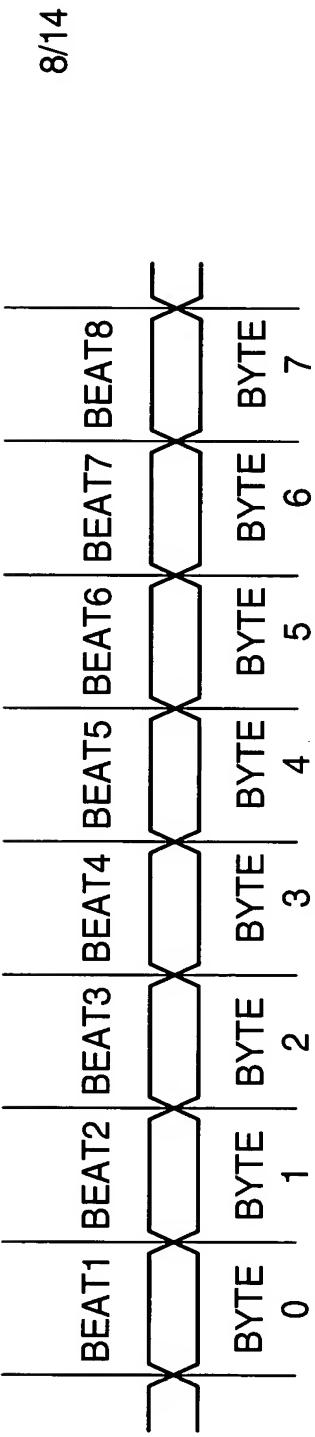


Fig. 8A

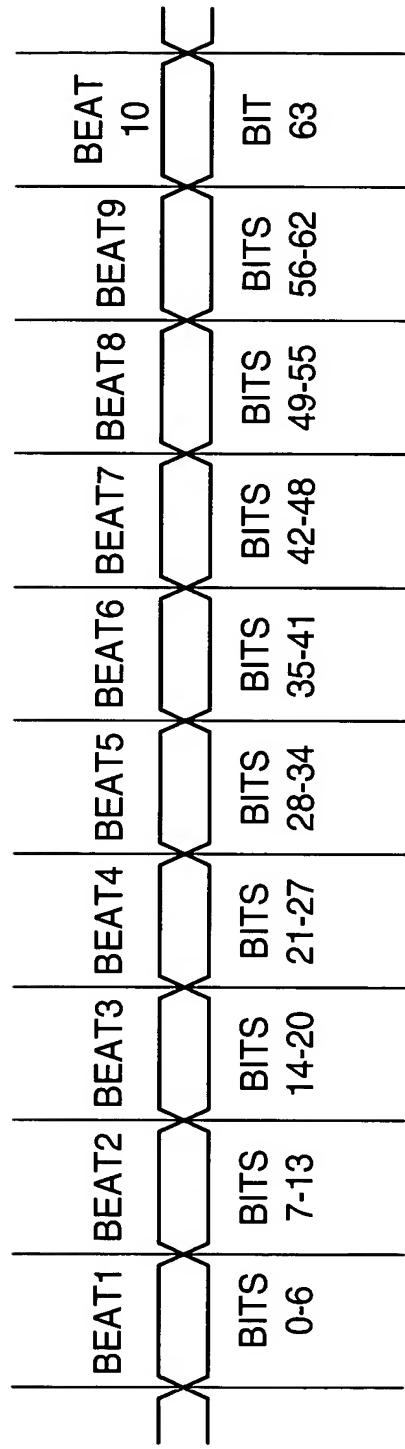


Fig. 8B

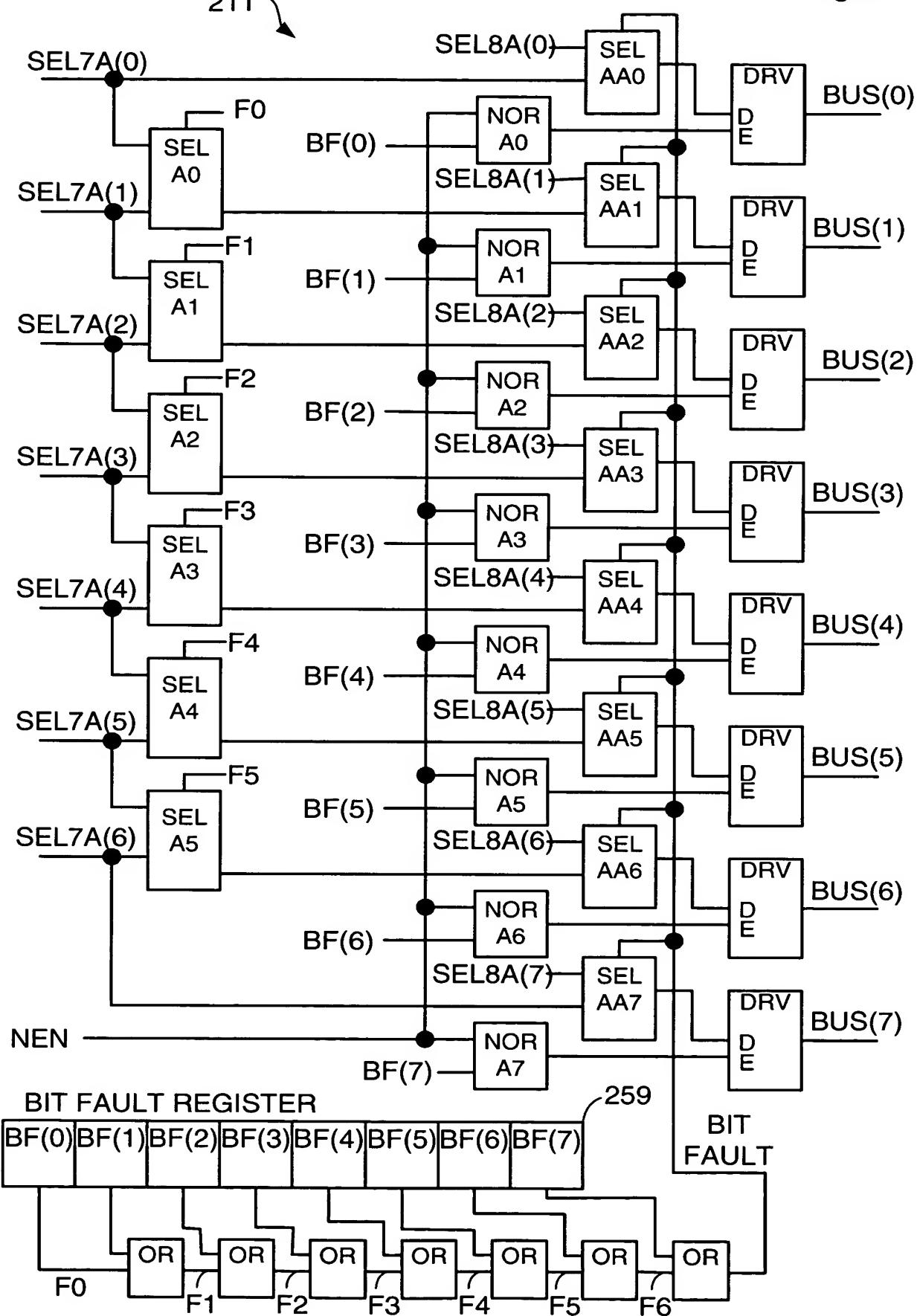
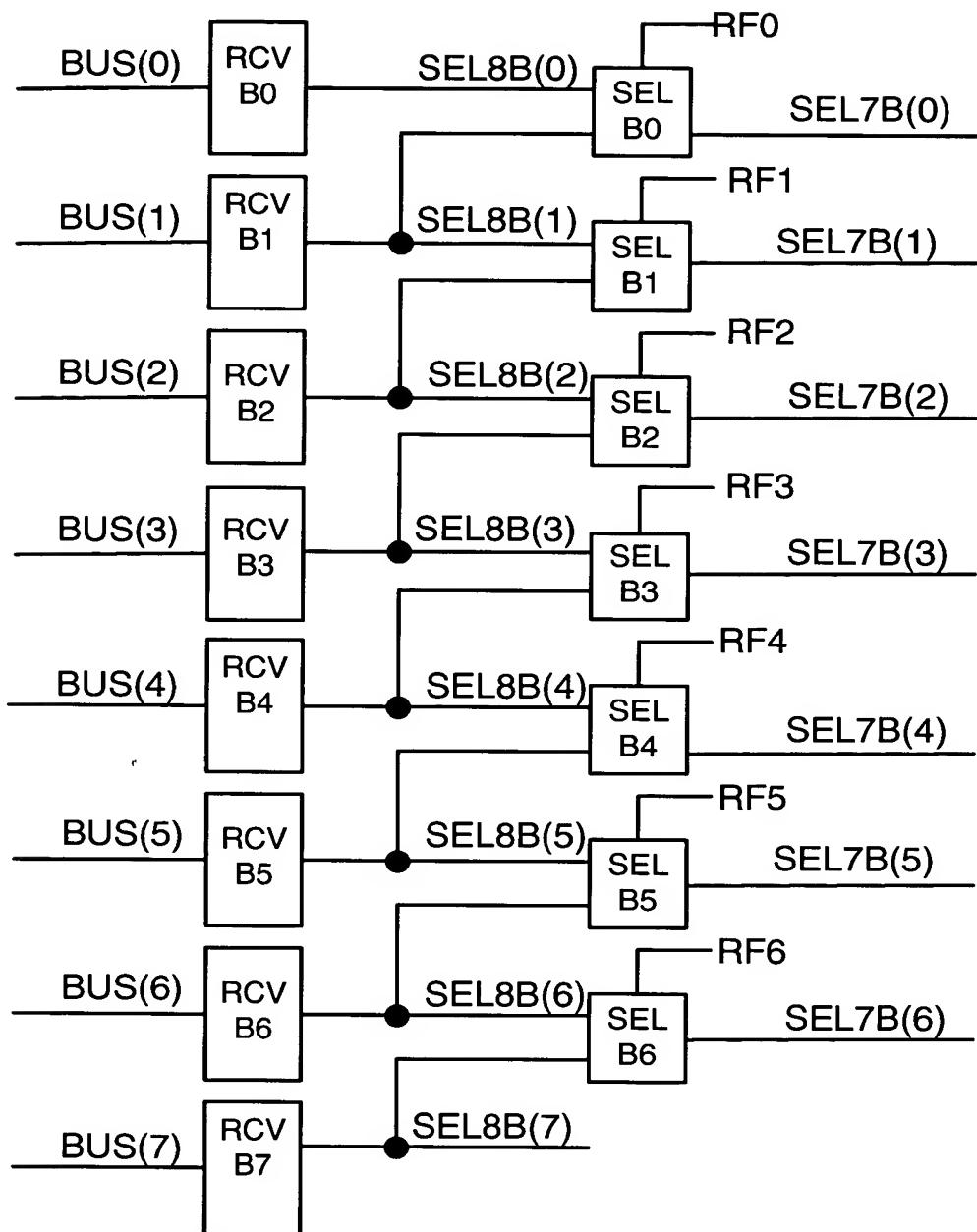


Fig. 10

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251



RECEIVE BIT FAULT REGISTER

260

292

RB _F (0)	RB _F (1)	RB _F (2)	RB _F (3)	RB _F (4)	RB _F (5)	RB _F (6)	RB _F (7)
------------------------	------------------------	------------------------	------------------------	------------------------	------------------------	------------------------	------------------------

RF0

RF1

RF2

RF3

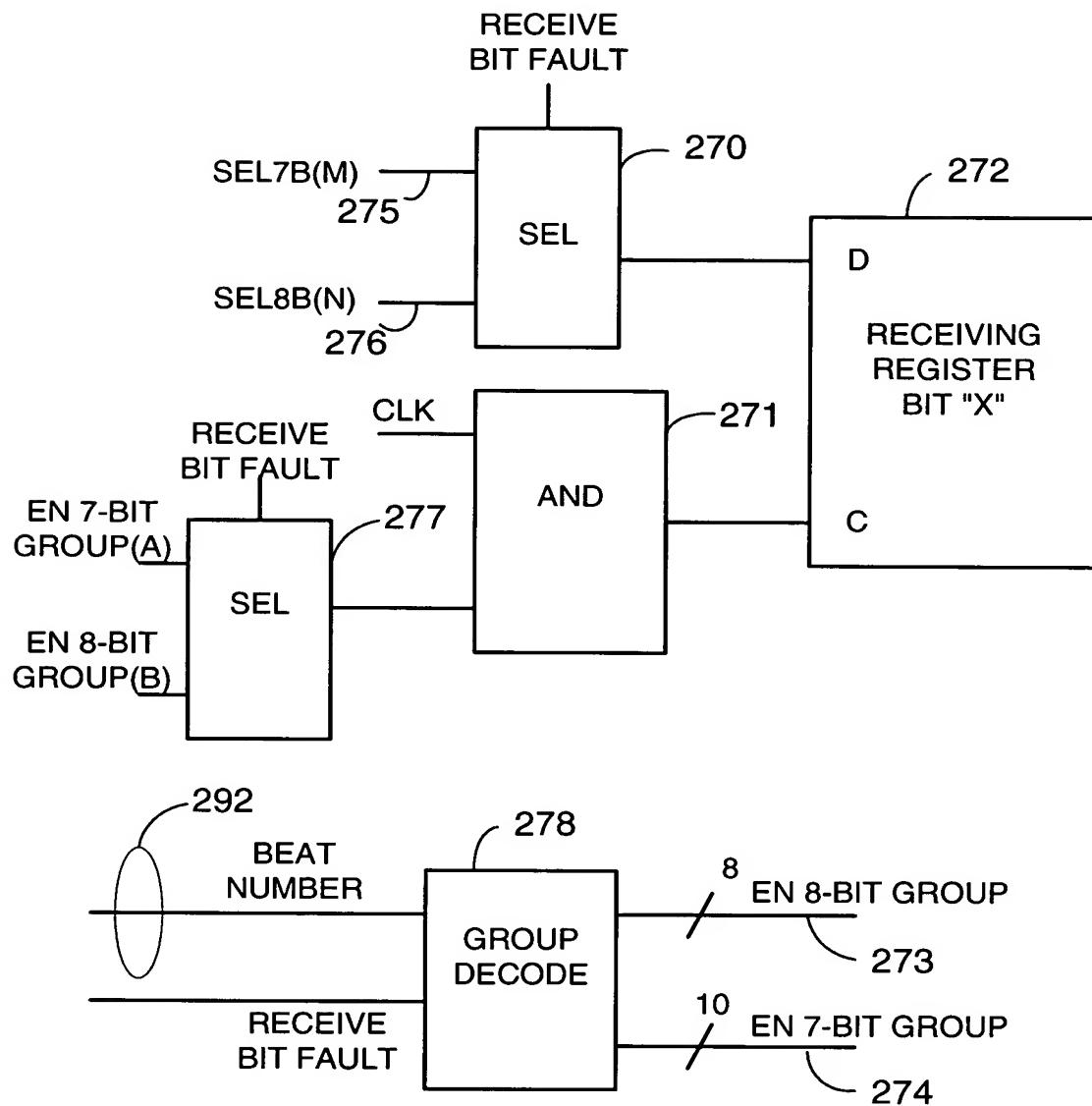
RF4

RF5

RF6

RECEIVE
BIT FAULT

Fig. 11



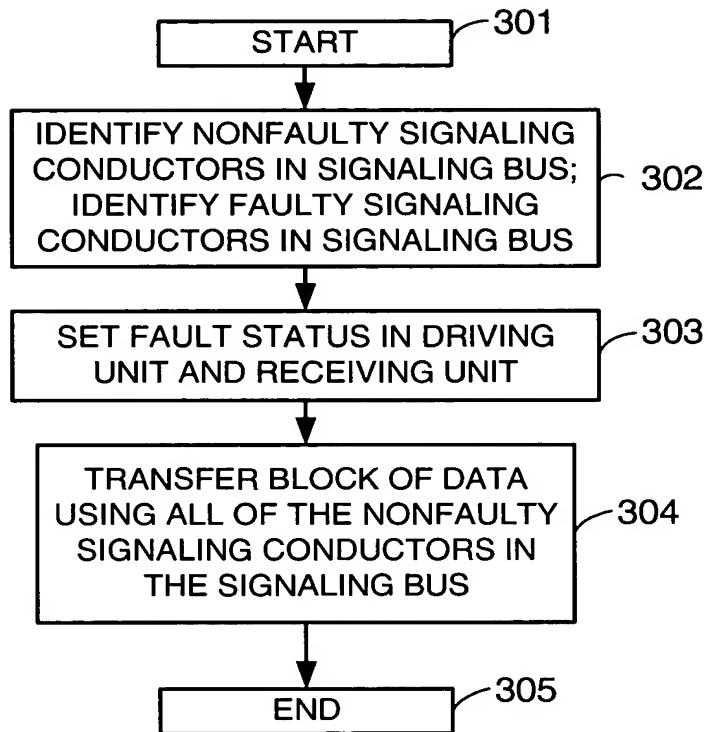


Fig. 12

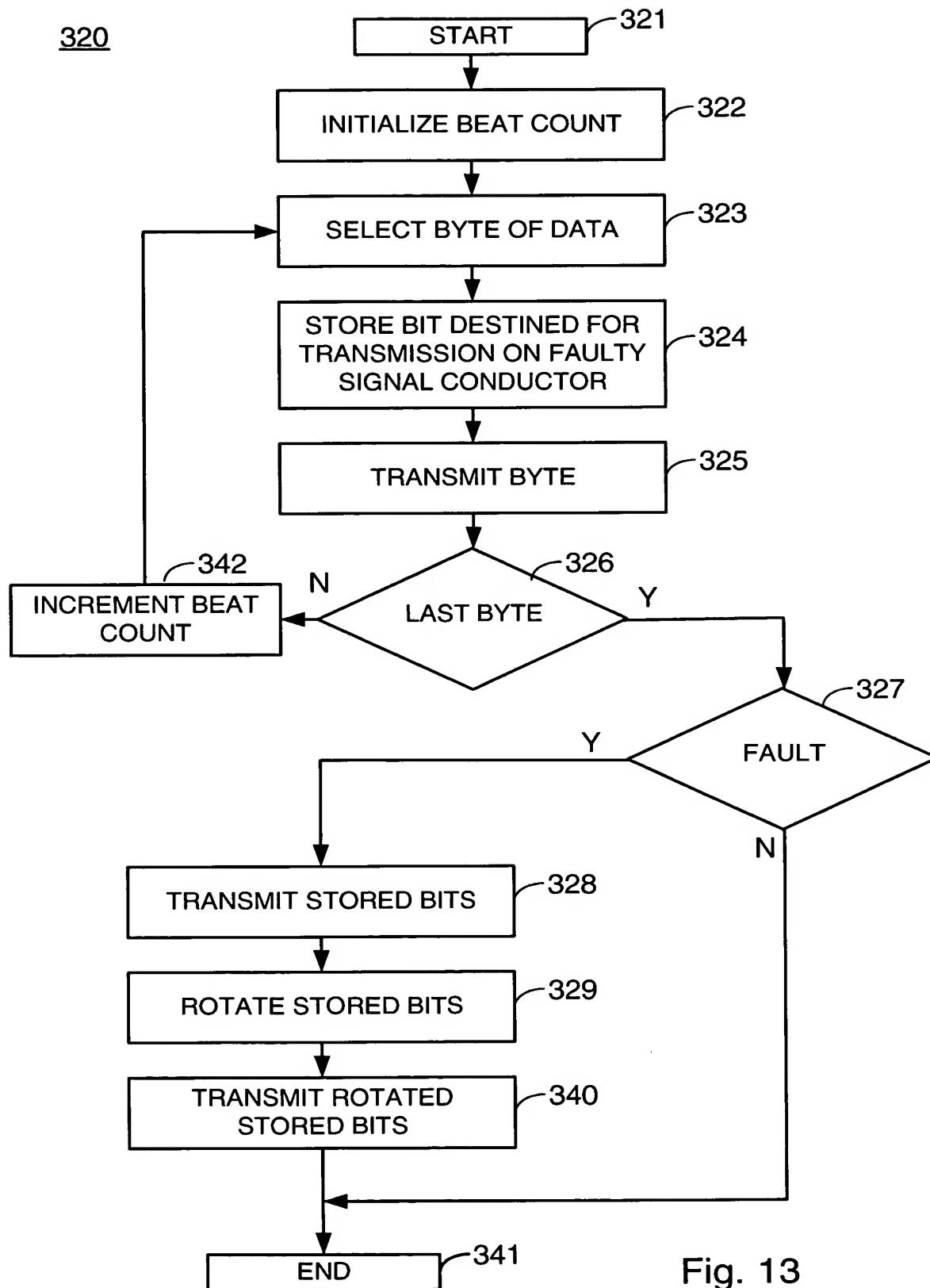


Fig. 13

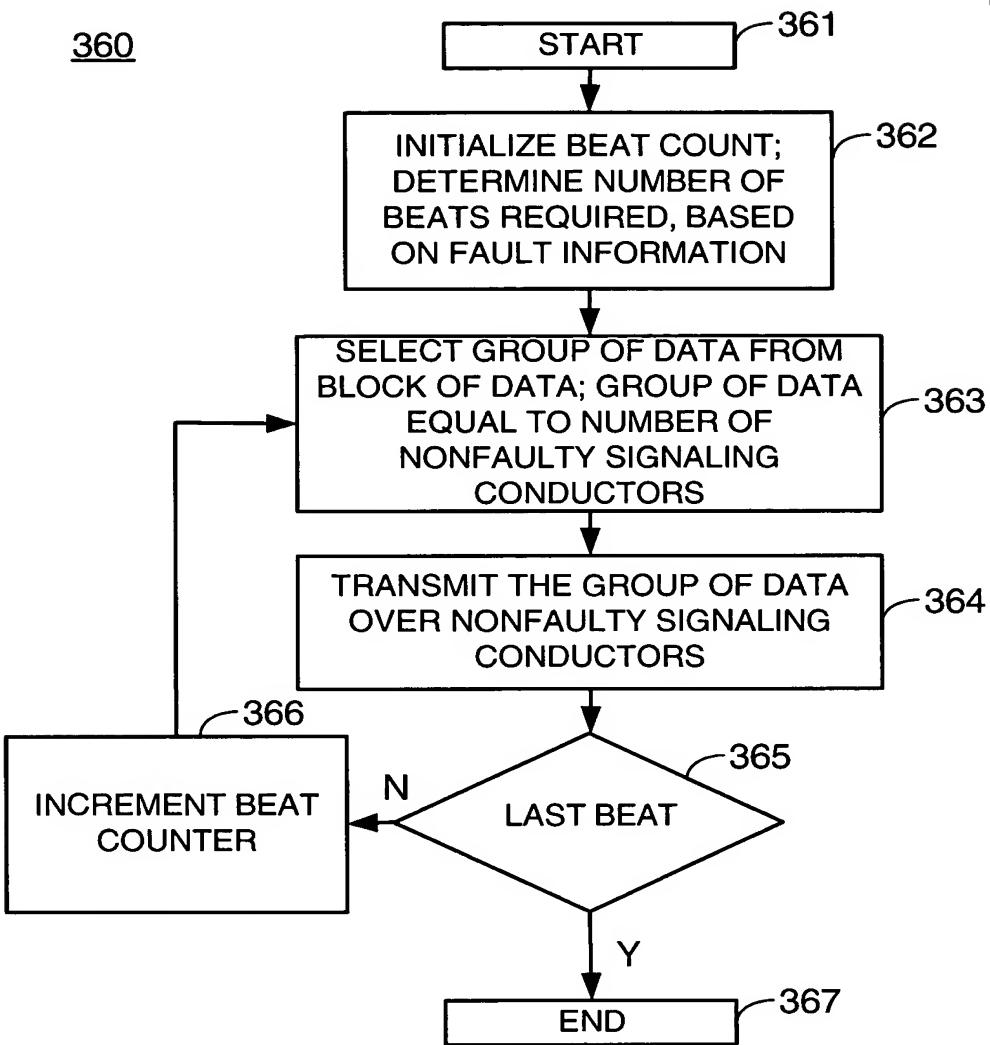


Fig. 14